Backends

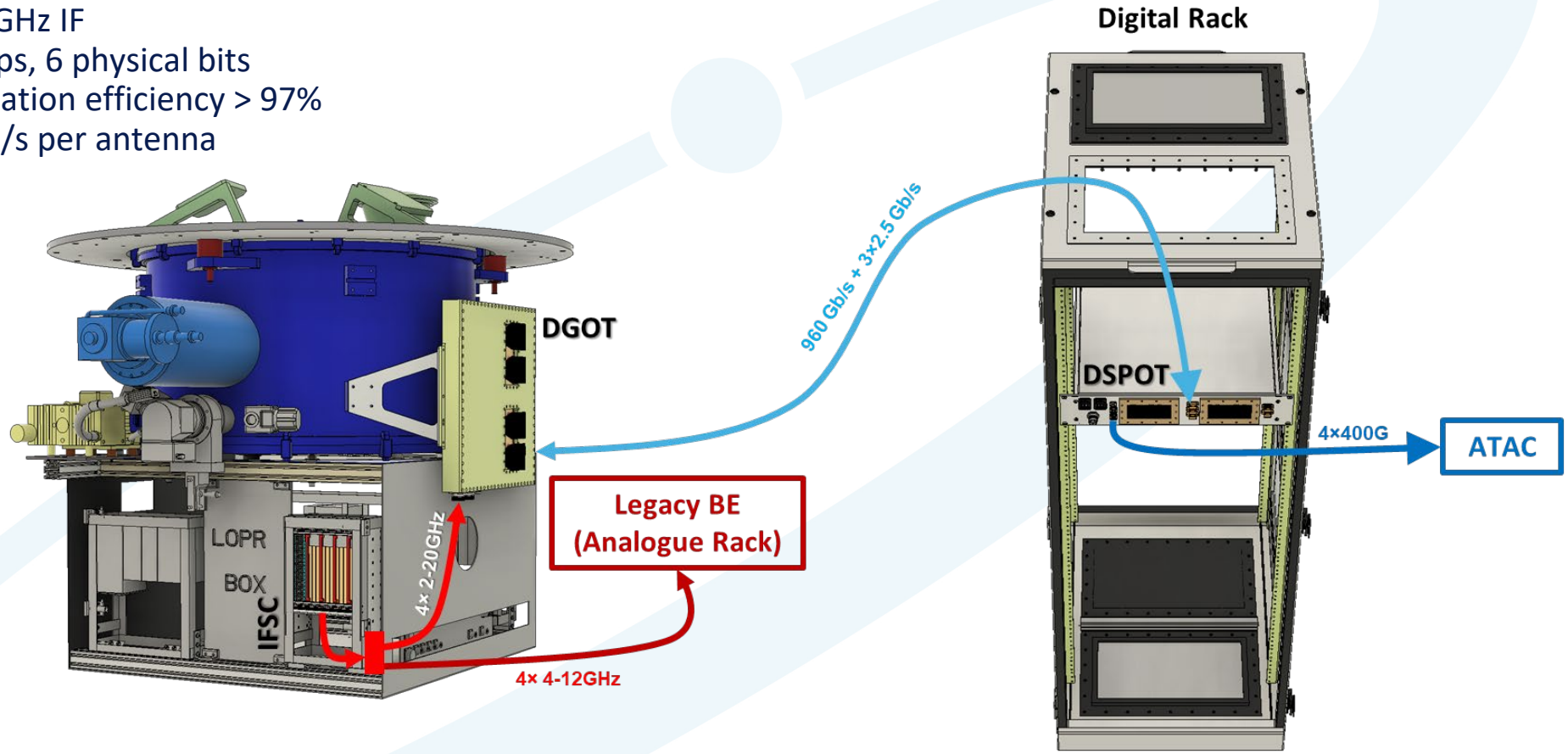
cnrs université de BORDEAUX

LABORATOIRE D'ASTROPHYSIQUE DE BORDEAUX

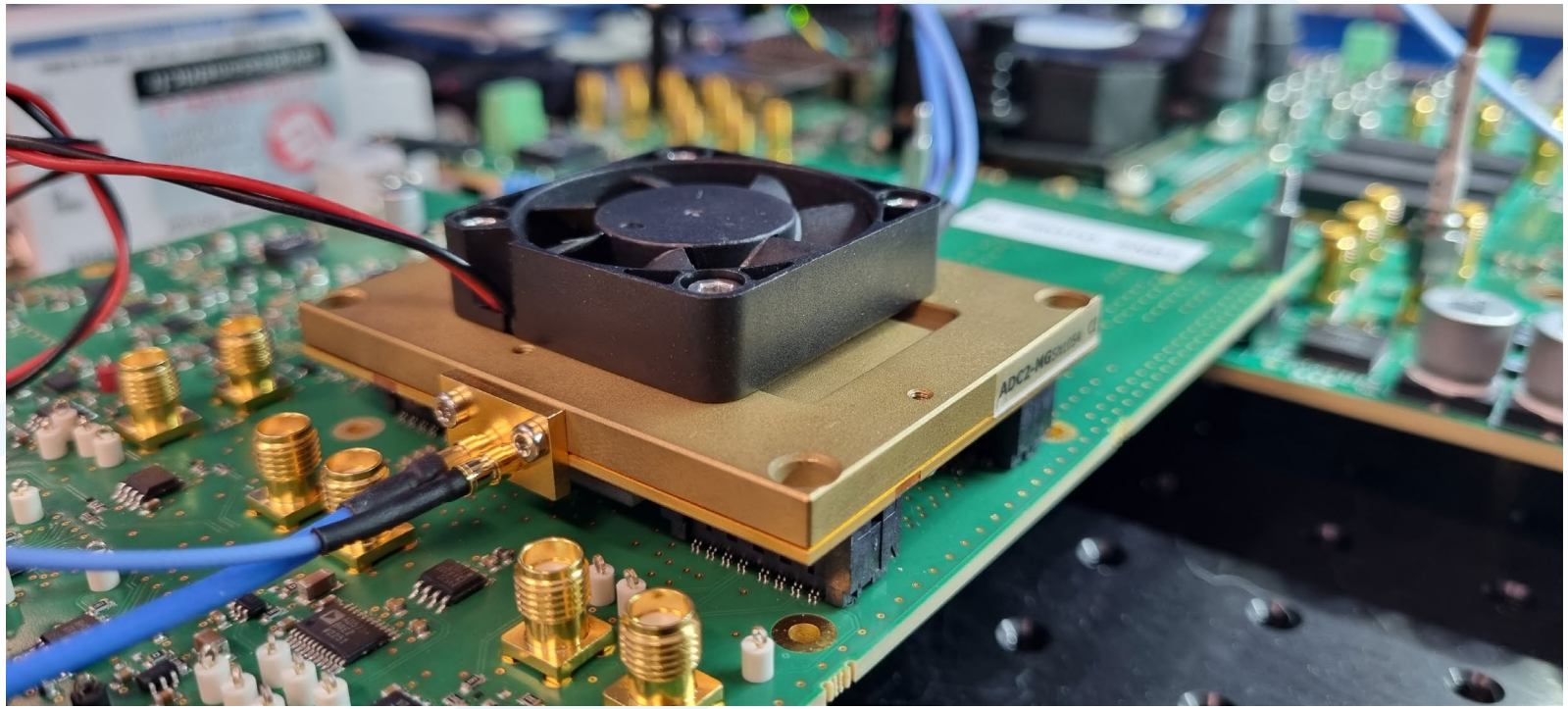
WIFP

WSU IF Processor

- Analog IF conditioning, digitization, Digital Signal Processing, and data transport
- ALMA WSU: increase bandwidth and sensitivity
- Direct digitization in one go
- Digital backend: higher versatility, stability, reproducibility
- 4*20 GHz IF
- 40 GSps, 6 physical bits
- Digitization efficiency > 97%
- 1.2 Tb/s per antenna



Digitization



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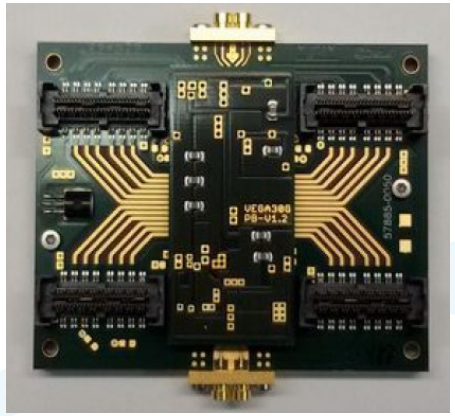
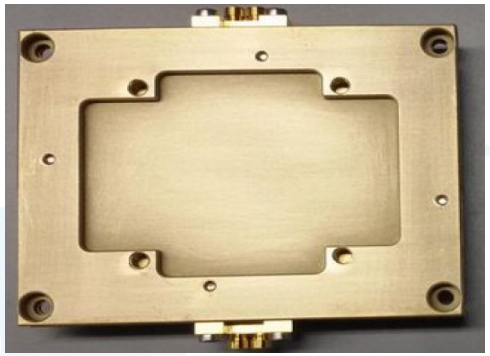
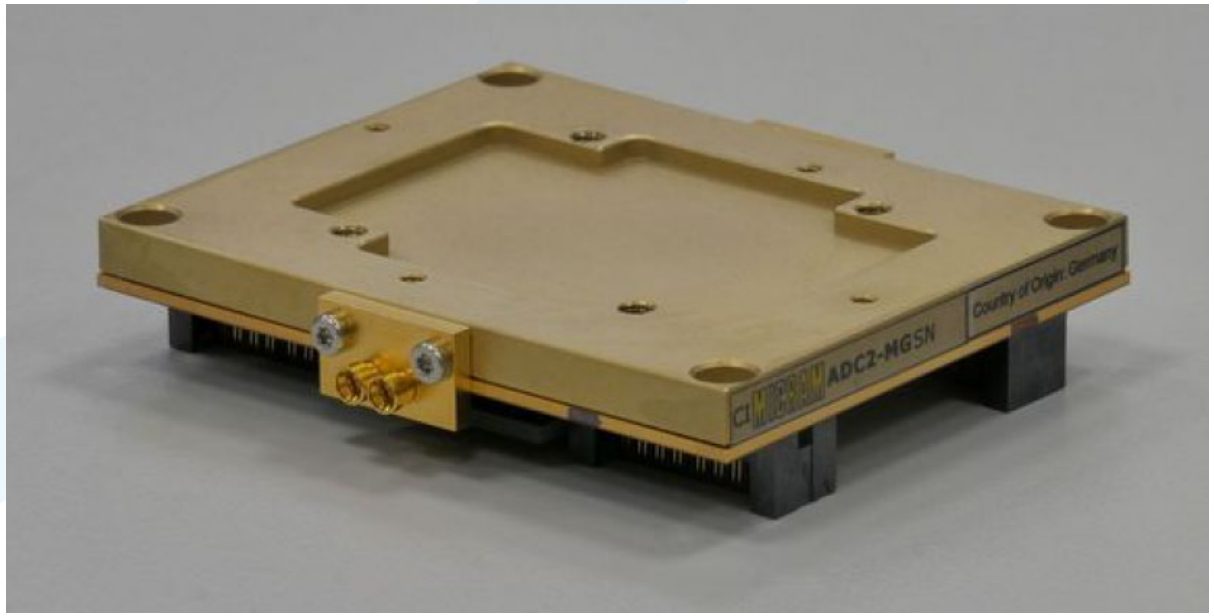


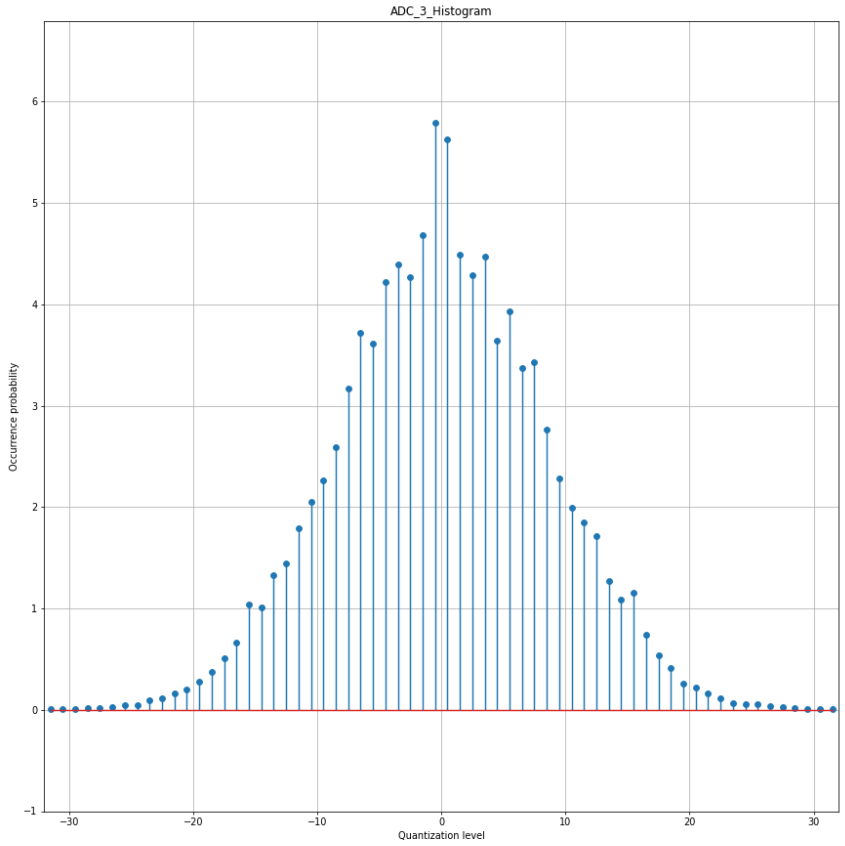


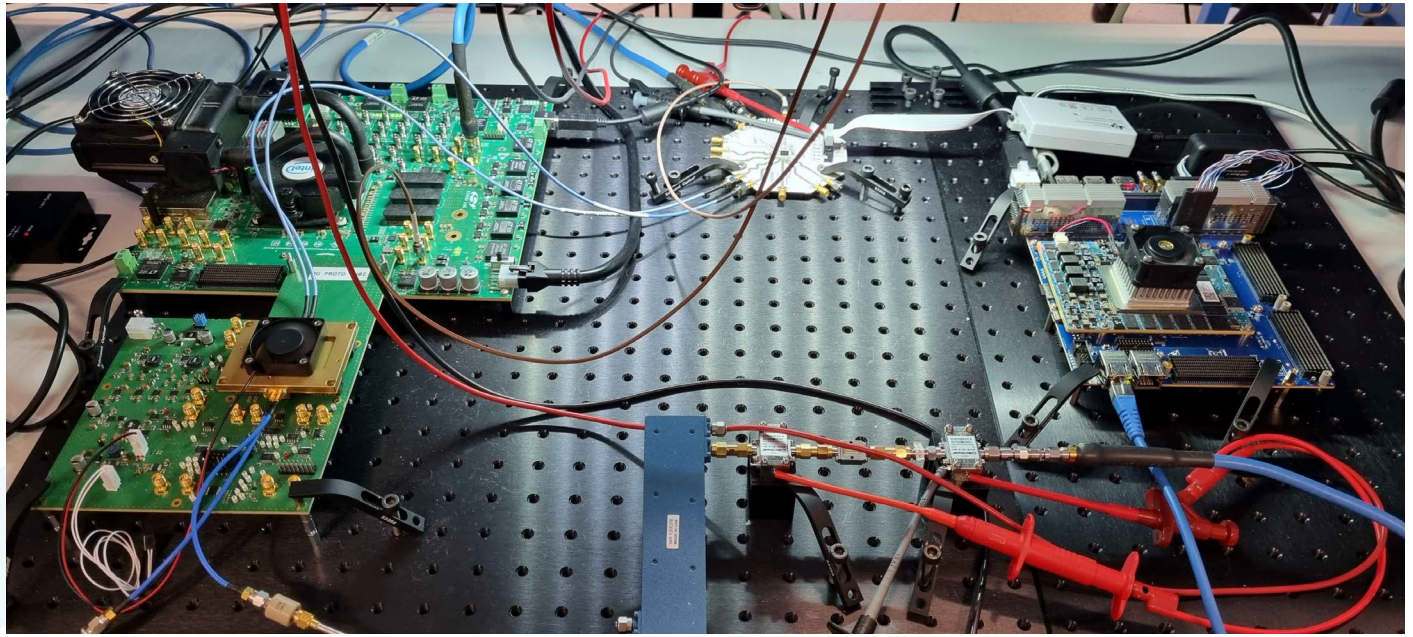
- High speed ADC (> 10 GSps)
  - Unsteady market, driven by military applications (radar)
  - Startups, big companies
  - Devices, IPs

- Baseline solution for WIFP: Micram ADC2-MG → Keysight M8130Y
  - 32 GSps – 6 bits
  - 4.5 ENOB for frequency < 20 GHz
  - 2 interleaved ADC based on flash folding interpolating architecture
  - SiGe bipolar chip, mounted on substrate, assembled on mechanical brass socket
  - Mini SMP connectors
  - Output interface: 4 de-multiplexed serial data lines
  - SONET PRBS synchronization / data scrambling
  - Typical power consumption: 10 W
  - Module temperature: 50°C
  - Cost: ~10 k€ for ~100 devices

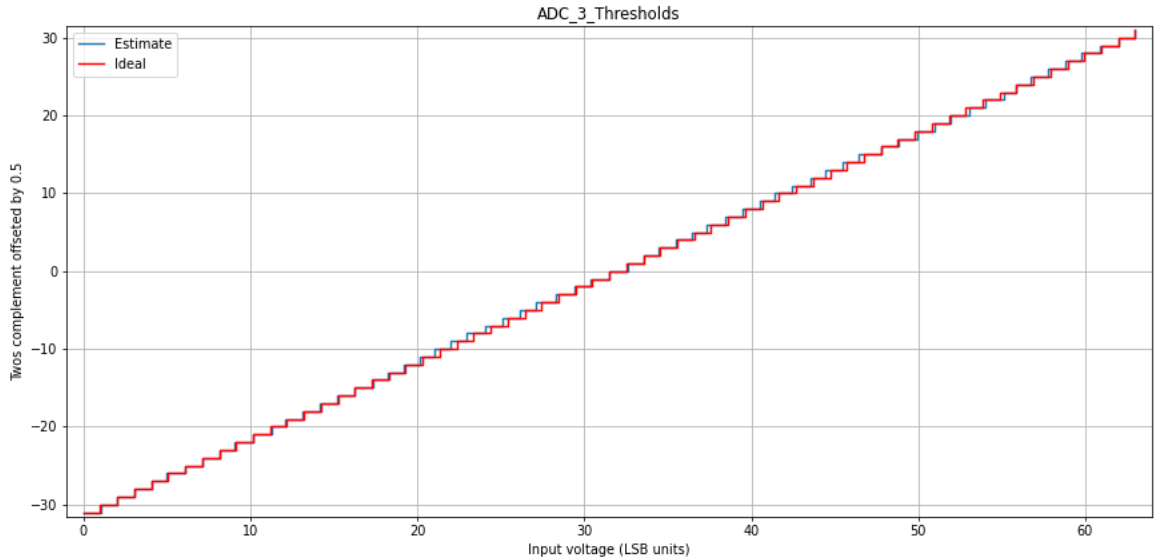


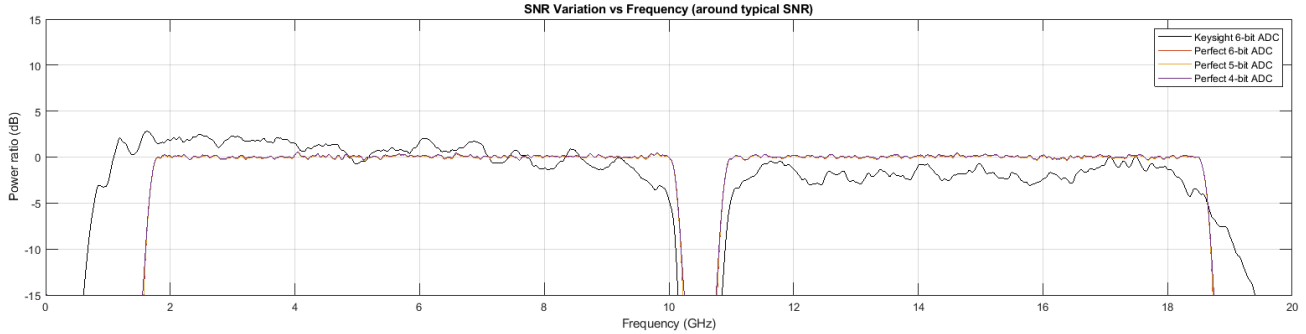
Digitization

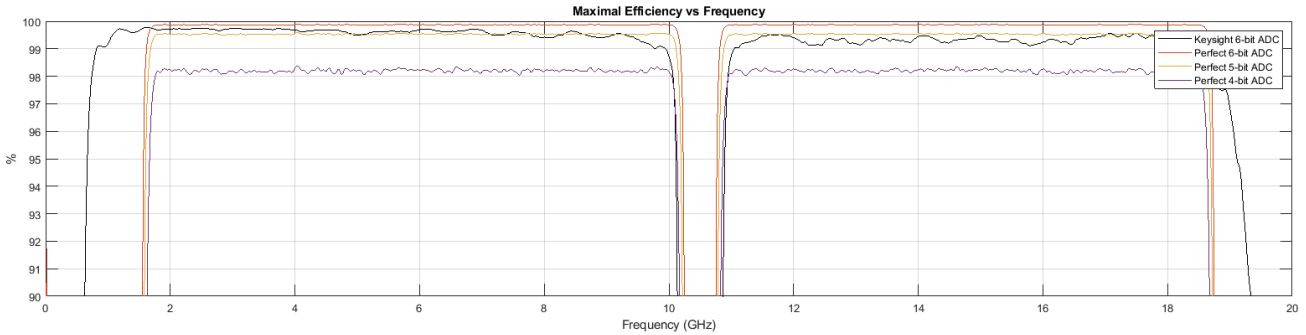


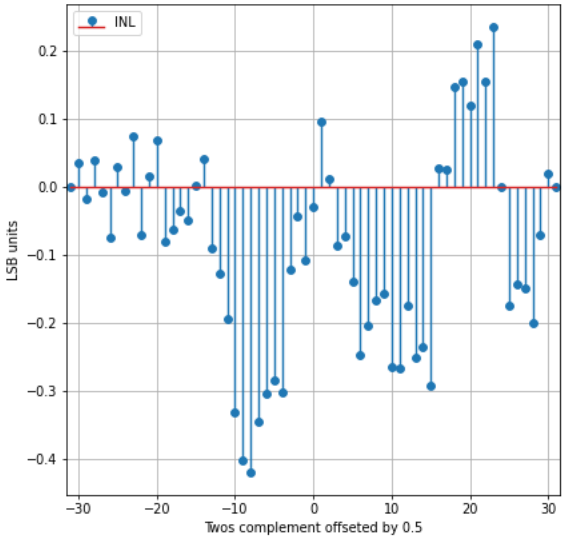


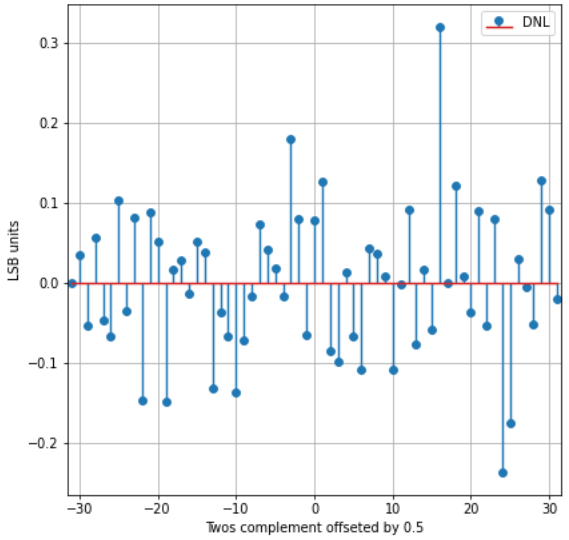
Digitization

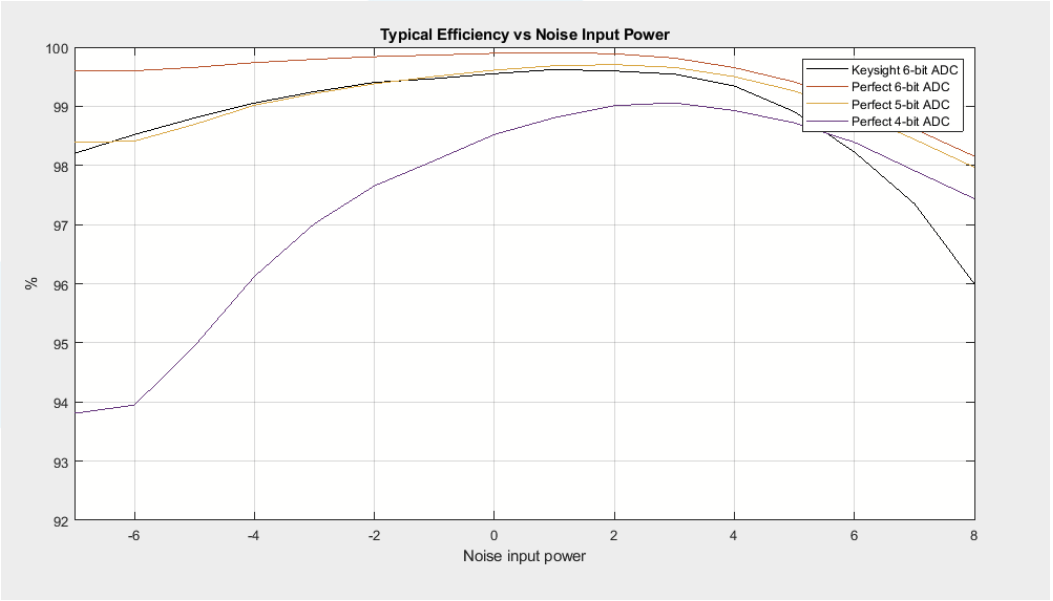












Digital Signal Processing

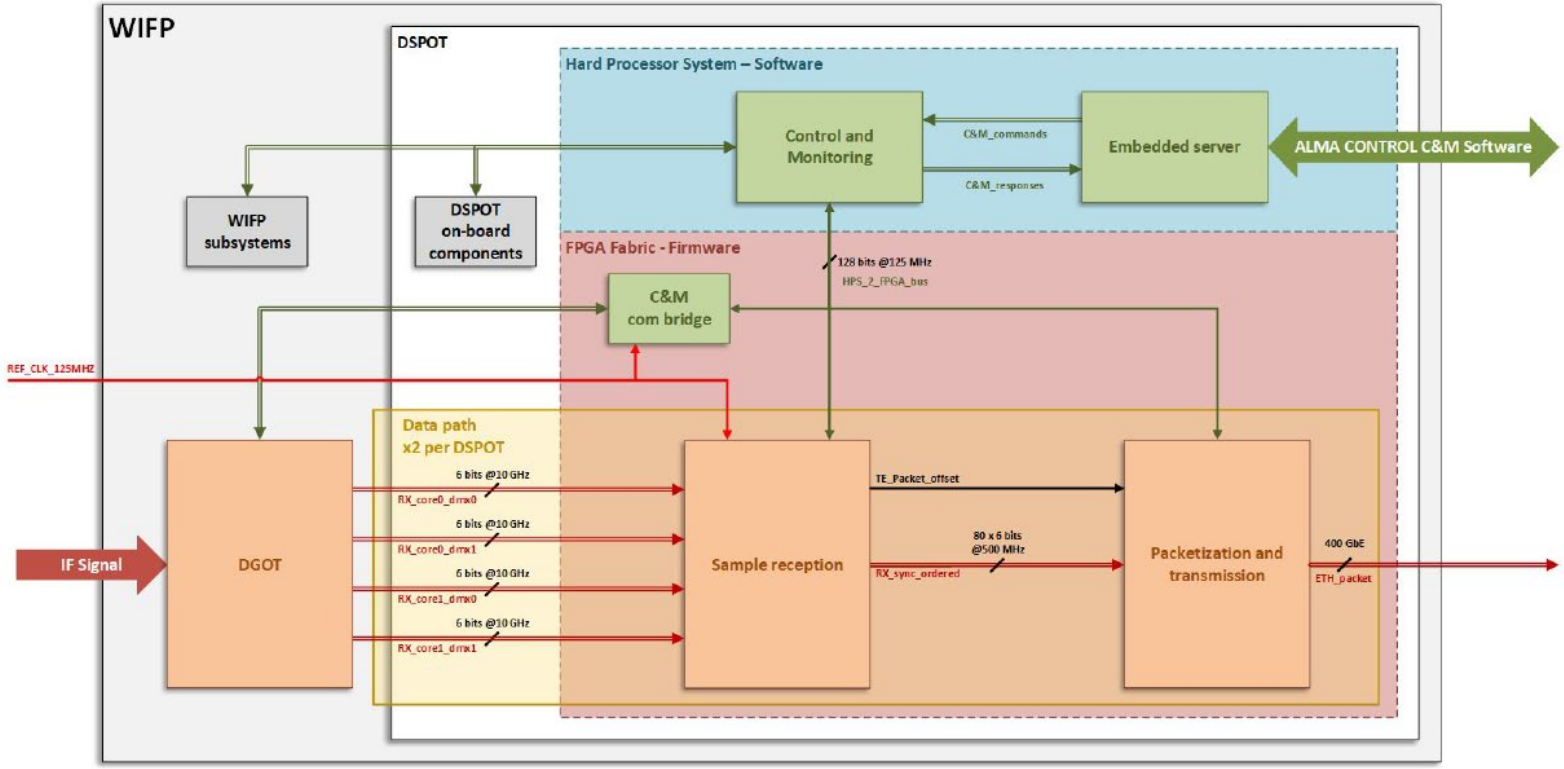
Digital Signal Processing

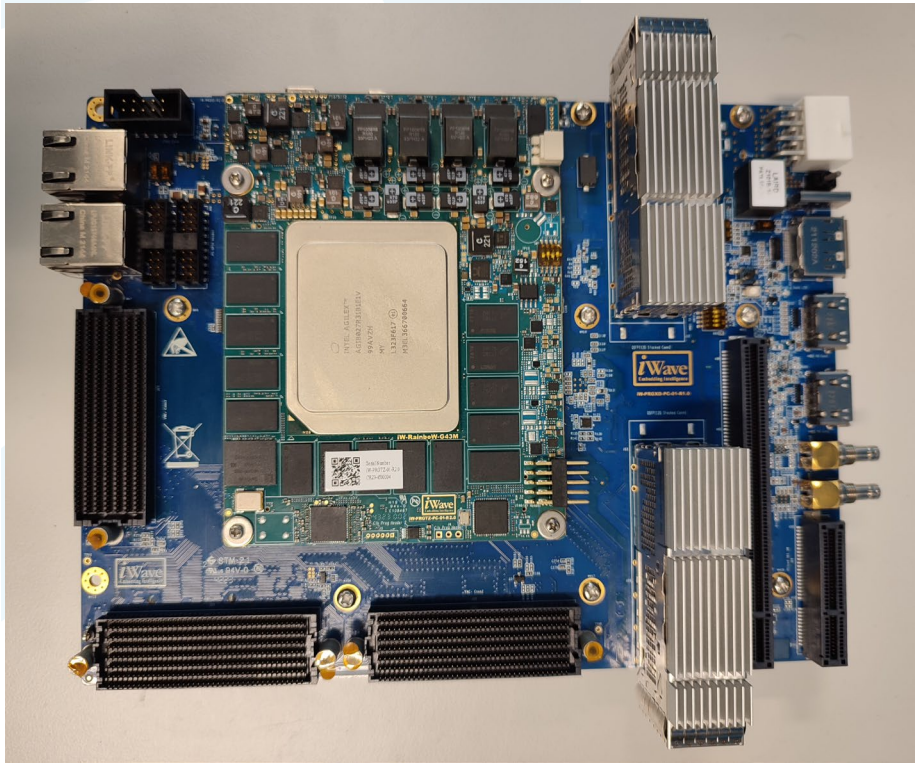
- FPGA
  - ADC interfacing (high speed transceivers are required)
  - FPGA selection driven by XCVR requirements
  - Control monitoring of external devices
  - “high speed / low level” DSP

- SoC (FPGA + embedded processor)
  - ARM uC used for:
    - High level control monitoring and sequencing
    - “low speed / high level” DSP
  - WIFP baseline solution: Altera Agilex-7 series, 10 nm
    - ADC interfacing
    - Time stamping (required because of non deterministic latency technologies/protocols)
    - Data packetization for transmission to the correlator through optical system with 400GbE

- System On Module available
  - Custom carrier board could be required to meet the specific instrument interface requirements
  - iWave SOM
    - Size: 120 mm × 90 mm
    - Cost: ~10 k€
    - Gigabit Ethernet, USB2.0, UART, SD, I2C, JTAG, SPI, I2C
    - High speed XCVRs and generic IOs
    - DDR4 memories
    - 12 V through B2B connector

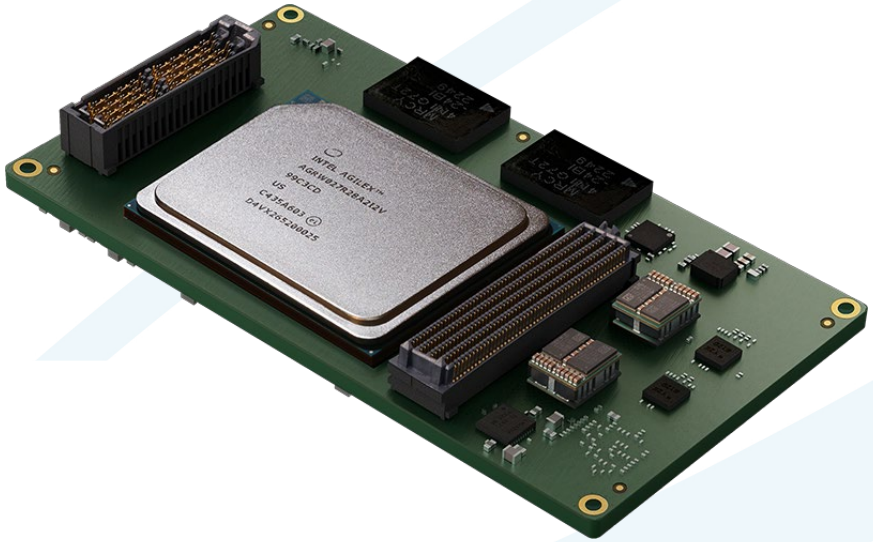
Digital Signal Processing

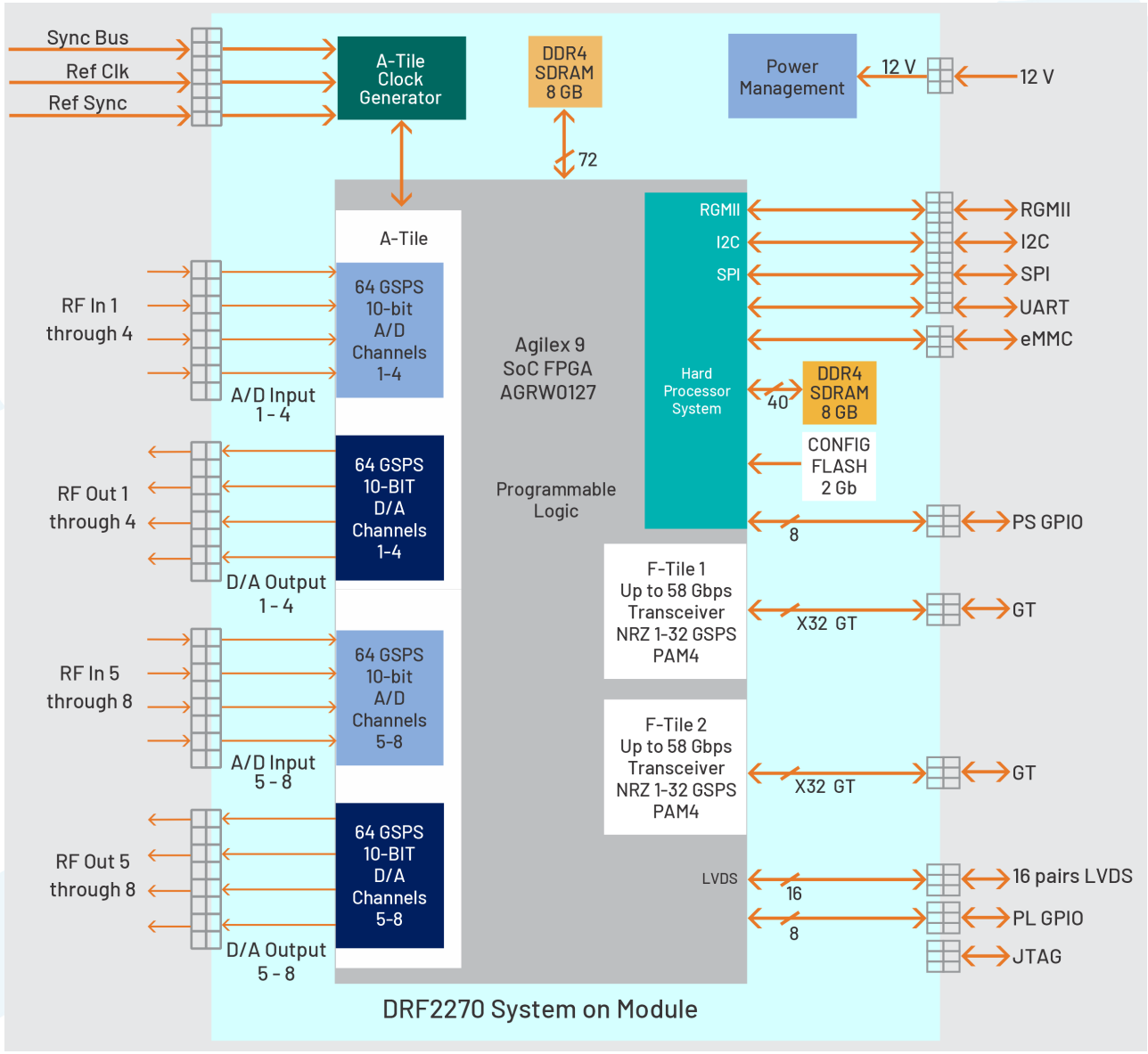


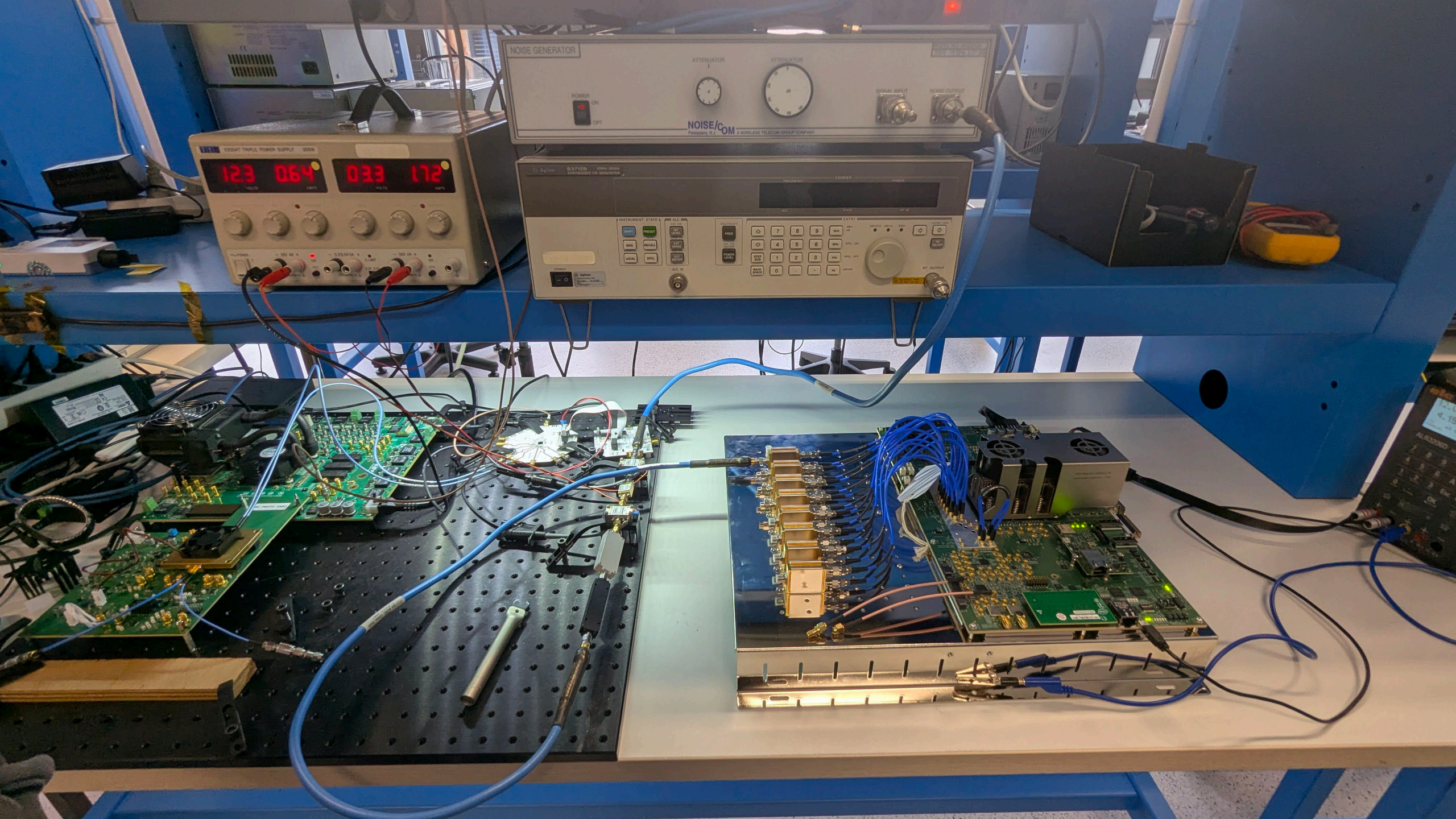


Digitization + DSP

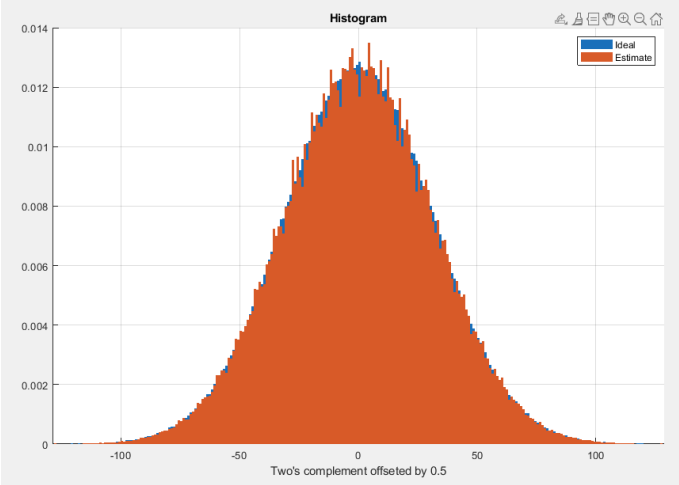
- Altera Agilex-9 direct-RF
  - 1 or 2 ADCs at 64 GSps with full bandwidth
  - 10 bits
  - High speed XCVRs for 400G links
  - RGMII interface for 10/100/1000 Ethernet
  - Cost: ~20 k€
- SOM already available
- DRF2270 from Mercury:
  - Size: 120.65 mm × 66.04 mm × 17.78 mm

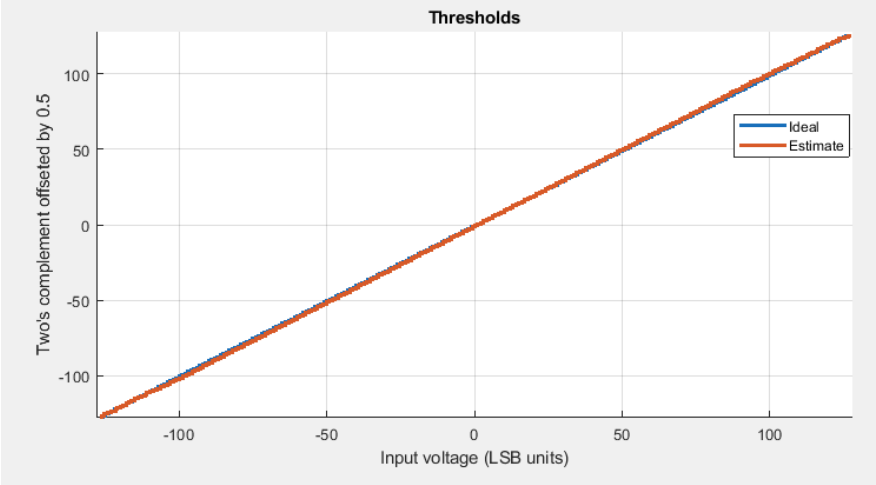


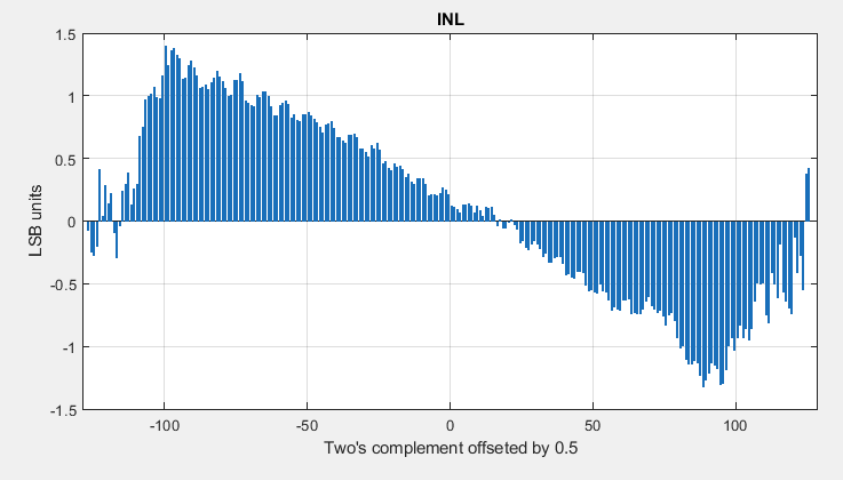


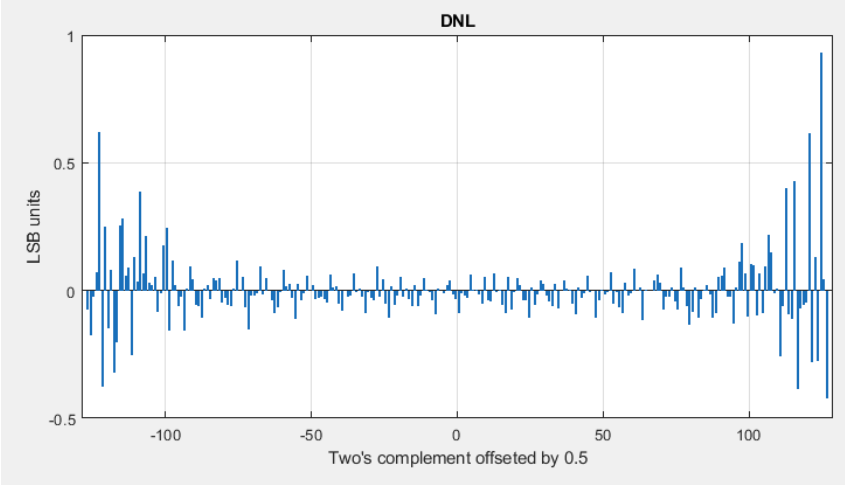

NOISE GENERATOR
NOISE/COM
123 064
033 172

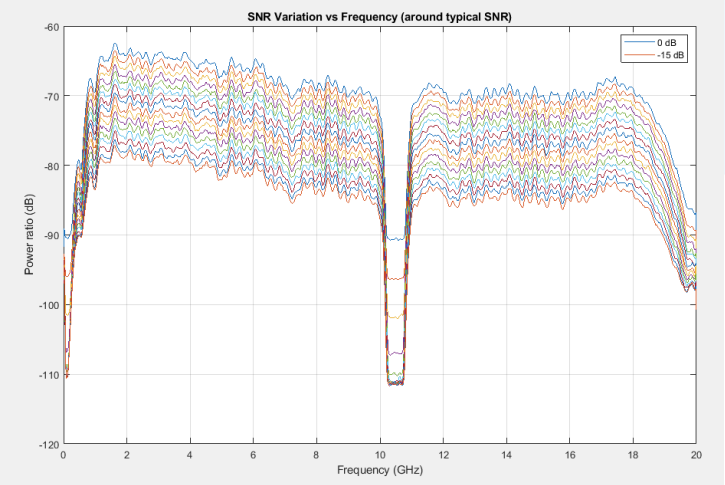
Direct-RF

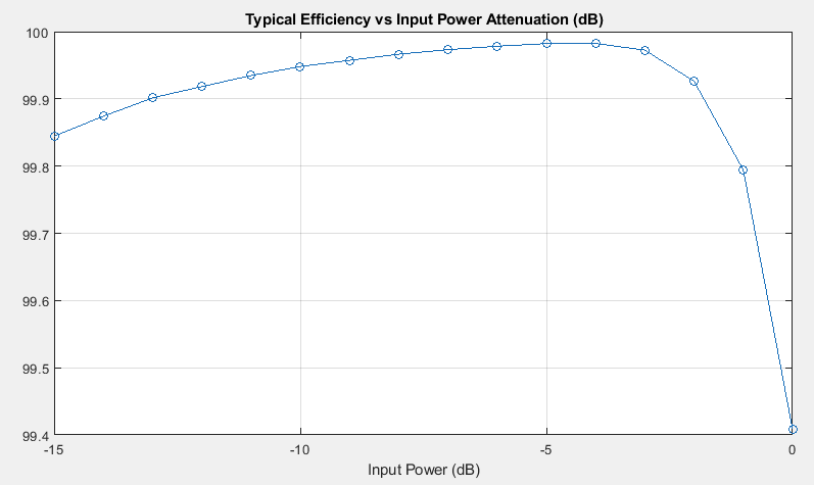

Histogram
Ideal
Estimate
Two's complement offseted by 0.5


Thresholds
Two's complement offseted by 0.5
Input voltage (LSB units)
Ideal
Estimate


INL
LSB units
Two's complement offseted by 0.5


DNL
LSB units
Two's complement offseted by 0.5


SNR Variation vs Frequency (around typical SNR)
0 dB
-15 dB
Power ratio (dB)
Frequency (GHz)


Typical Efficiency vs Input Power Attenuation (dB)
Input Power (dB)

Direct-RF

- Measurements performed with 8 bits
  - 2 LSB are not available with the specific dynamically reconfigurable FW used by Altera for this demo
  - A different FW with 10 bits is available and could be used for another test campaign
- Exact same RF chain used as for the Keysight test campaign
- Captured samples are processed with Matlab LAB codes

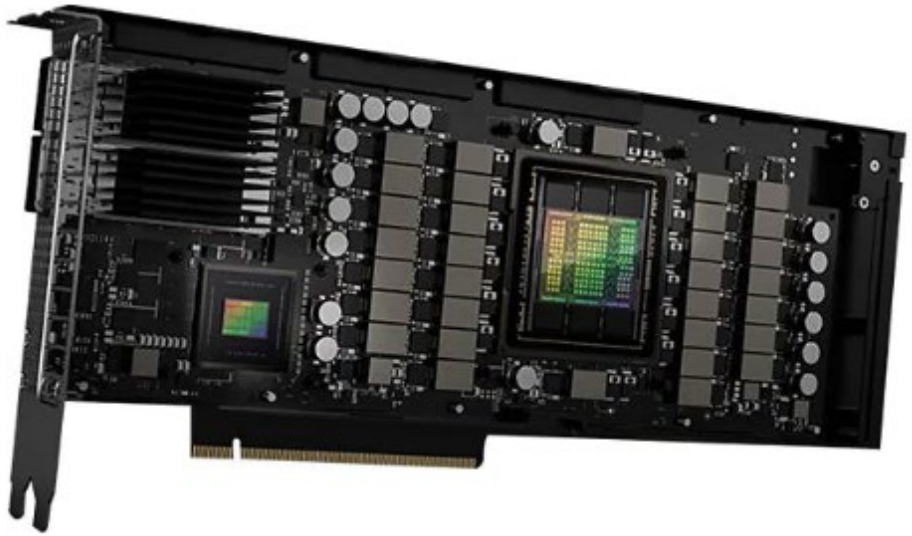
- Efficiency at -5 dB (no clipping & best efficiency):
  - Maximal Efficiency = 99.995%
  - Typical Efficiency = 99.982%
  - Minimal Efficiency = 99.962%
- NPR = 6.02*ENOB + cst → ENOB direct-RF = ENOB Keysight + 2.5

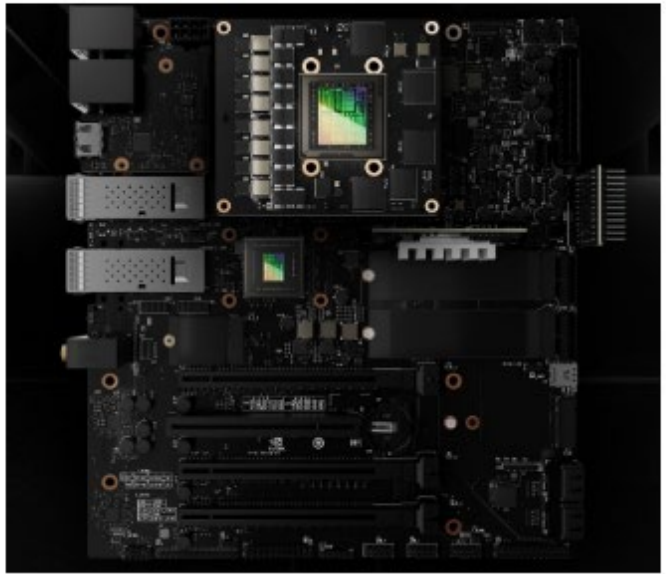
- Power consumption:
  - 7 W (one RFSoC ADC) vs 27W = 10 W (one Keysight ADC) + 17 W (12 FPGA XCVR)
  - 28 W vs 108 W per antenna

Digital Signal Processing

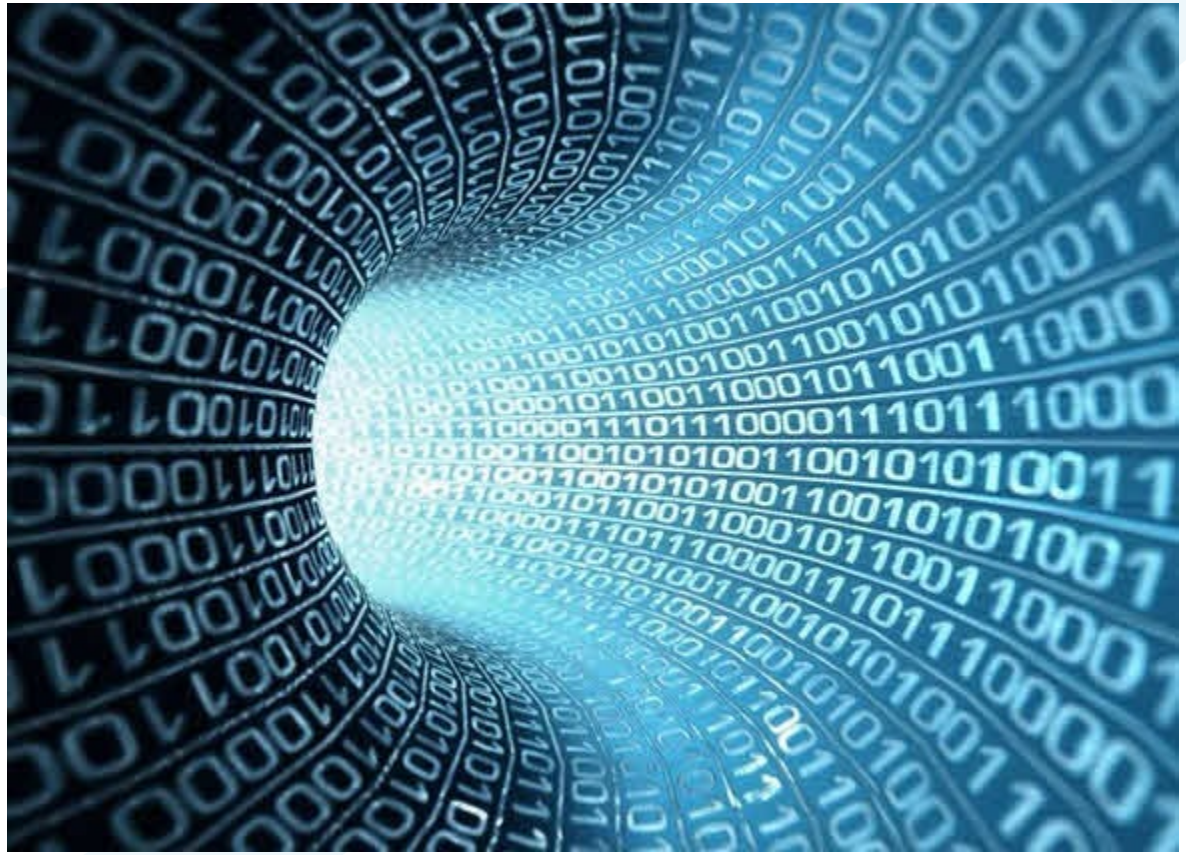
- GPU
  - “high speed / intermediate level” DSP
  - ESO/NAOJ GPU study, ALMA TPGS
  - WIFP test equipment
- Next gen GPU:
  - H100 CNX, IGX Orin, Grace Hopper superchip
  - ~50 k€ for one GPU
  - ~500W

Component	Estimated Cost (USD)
Base Chassis/Platform	$30,000
CPUs (dual-socket EPYC Gen5, ~32-core each)	$6,000–$7,000
NICs (2× 400 GbE)	$20,000
GPUs (2× H100/Grace Hopper)	$130,000–$160,000
Memory (e.g. 512 GB DDR5)	$2,000–$4,000
NVMe Storage (OS + scratch)	$1,500–$2,000
Ancillary/Integration	$5,000–$10,000
Subtotal	$194,500–$233,000
Plus ~15% Overhead	$29,200–$35,000
Total Estimated Cost	$223,700–$268,000



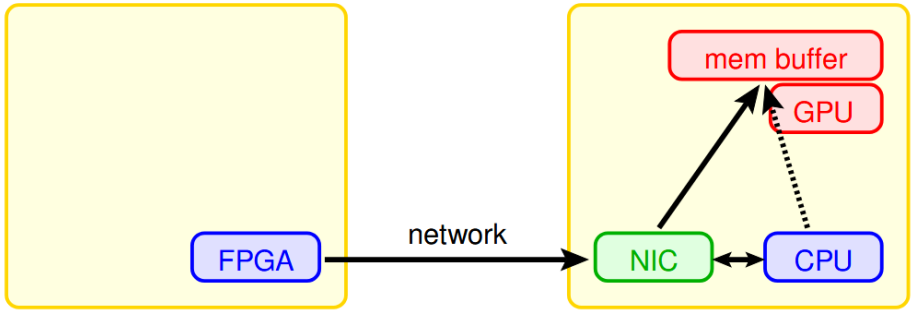


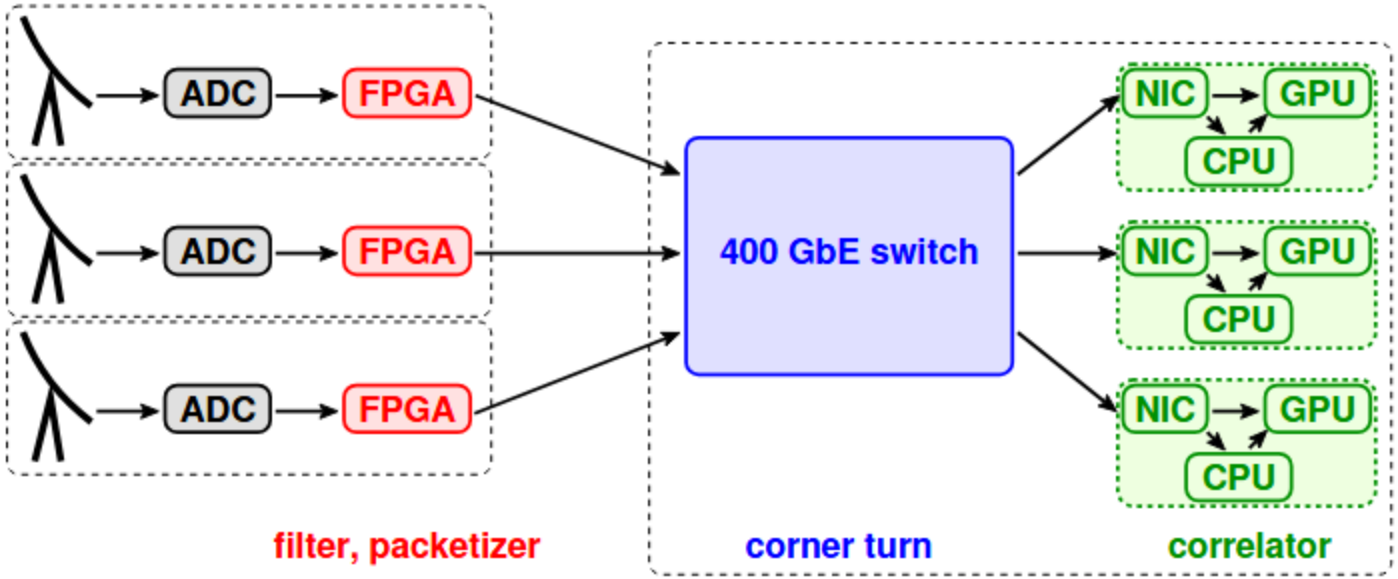
Data Transport



Data transport

- IOs must scale proportionally to digitization and DSP capabilities
- From ADC to FPGA: standard protocols, custom, FPGA XCVRs
- From FPGA to FPGA: 100/200/400 GbE IP
- From FPGA to GPU
- EU funded Horizon Radioblocks project
- WP4: data transport and correlation
- Beyond ~10GSps: prohibitive OS overheads (interrupts, copying, etc.)
- New solutions required: RDMA, DPDK, DOCA
- Stream data directly from FPGA to GPU
- Packet header → CPU
- Packet payload → GPU





Takeout

- Digitization
  - Direct digitization = less analog parts, higher versatility, stability, reproducibility
  - Very few high speed, wide band, ADC (> 10 GSps, 10 GHz)
    - multi-cores, complex architectures
    - calibration (CW vs Gaussian noise)

- DSP
  - Integration of soft and hard IPs in state of the art FPGA
  - System on Chip = FPGA + Hard Processor System
  - Direct-RF = FPGA/SoC + ADC/DAC
  - System on Module = FPGA + generic surrounding functions/devices on a small form factor PCB

- Data transport
  - From ADC to FPGA = XCVR (standard or custom protocols)
  - From FPGA to FPGA = 100/200/400 GbE
  - From FPGA to GPU = need to bypass CPU for data transfer